

FEATURES

Low input bias current

- ±20 fA maximum at $T_A = 25^\circ\text{C}$ (guaranteed at production test)
- ±20 fA maximum at $-40^\circ\text{C} < T_A < +85^\circ\text{C}$
- ±250 fA maximum at $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ (guaranteed at production test)

Low offset voltage: 50 μV maximum over specified CMRR range

Offset voltage drift: ±0.13 $\mu\text{V}/^\circ\text{C}$ typical, ±0.5 $\mu\text{V}/^\circ\text{C}$ maximum

Integrated guard buffer with 100 μV maximum offset

Low voltage noise density: 14 nV/ $\sqrt{\text{Hz}}$ at 10 kHz

Wide bandwidth: 2 MHz unity-gain crossover

Supply voltage: 4.5 V to 16 V (±2.25 V to ±8 V)

Operating temperature: -40°C to $+125^\circ\text{C}$

Long-term offset voltage drift (10,000 hours): 0.5 μV typical

Temperature hysteresis: 1.5 μV typical

APPLICATIONS

Laboratory and analytical instrumentation: spectrophotometers, chromatographs, mass spectrometers, and potentiostatic and amperostatic coulometry

Instrumentation: picoammeters and coulombmeters

Transimpedance amplifier (TIA) for photodiodes, ion chambers, and working electrode measurements

High impedance buffering for chemical sensors and capacitive sensors

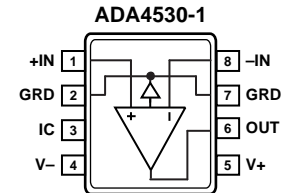
GENERAL DESCRIPTION

The ADA4530-1 is a femtoampere (10^{-15} A) level input bias current operational amplifier suitable for use as an electrometer that also includes an integrated guard buffer. It has an operating voltage range of 4.5 V to 16 V, enabling it to operate in conventional 5 V and 10 V single supply systems as well as ±2.5 V and ±5 V dual supply systems.

It provides ultralow input bias currents that are production tested at 25°C and at 125°C to ensure the device meets its performance goals in user systems. The integrated guard buffer isolates the input pins from leakage in the printed circuit board (PCB), minimizes board component count, and enables easy system design. The ADA4530-1 is available in an industry-standard surface-mount 8-lead SOIC package with a unique pinout optimized to prevent signals from coupling between the sensitive input pins, the power supplies, and the output pin while enabling easy routing of the guard ring traces.

The ADA4530-1 also offers low offset voltage, low offset drift, and low voltage and current noise needed for the types of applications that require such low leakages.

PIN CONNECTION DIAGRAM



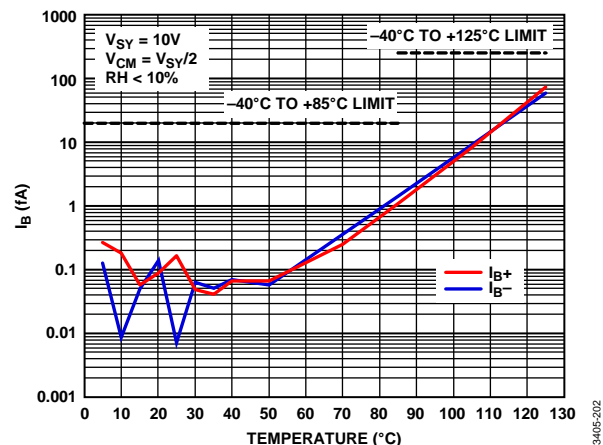
NOTES
1. IC = INTERNAL CONNECTION. THIS PIN MUST BE CONNECTED TO V- OR LEFT UNCONNECTED.

13405-001

Figure 1.

To maximize the dynamic range of the system, the ADA4530-1 has a rail-to-rail output stage that can typically drive to within 30 mV of the supply rails under a 10 k Ω load.

The ADA4530-1 operates over the -40°C to $+125^\circ\text{C}$ industrial temperature range and is available in an 8-lead SOIC package.


 Figure 2. Input Bias Current (I_b) vs. Temperature, $V_{SY} = 10$ V

Rev. B

Document Feedback

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

Features	1	Input Resistance.....	34
Applications.....	1	Input Offset Voltage.....	34
Pin Connection Diagram	1	Insulation Resistance	34
General Description	1	Guarding.....	35
Revision History	3	Dielectric Relaxation.....	35
Specifications.....	4	Humidity Effects.....	37
5 V Nominal Electrical Characteristics	4	Contamination.....	38
10 V Nominal Electrical Characteristics	6	Cleaning and Handling	39
15 V Nominal Electrical Characteristics	8	Solder Paste Selection	39
Absolute Maximum Ratings.....	10	Current Noise Considerations	40
Thermal Resistance	10	Layout Guidelines.....	43
ESD Caution.....	10	Physical Implementation of Guarding Techniques.....	43
Pin Configuration and Function Descriptions.....	11	Guard Ring.....	43
Typical Performance Characteristics	12	Guard Plane.....	43
Main Amplifier, DC Performance.....	12	Via Fence	44
Main Amplifier, AC Performance	21	Cables and Connectors.....	44
Guard Amplifier	27	Electrostatic Interference	44
Theory of Operation	29	Photodiode Interface.....	45
ESD Structure.....	29	DC Error Analysis.....	45
Input Stage.....	29	AC Error Analysis	45
Gain Stage	30	Noise Analysis.....	46
Output Stage.....	30	Design Recommendations	47
Guard Buffer	30	Design Example	47
Applications Information	31	Power Supply Recommendations.....	50
Input Protection.....	31	Power Supply Considerations.....	50
Single-Supply and Rail-to-Rail Output	31	Long-Term Drift.....	51
Capacitive Load Stability	31	Temperature Hysteresis	51
EMI Rejection Ratio.....	32	Outline Dimensions	52
High Impedance Measurements.....	33	Ordering Guide	52
Input Bias Current	33		

REVISION HISTORY

5/2017—Rev. A to Rev. B

Changes to Features Section and General Description Section 1
 Changed Offset Voltage Parameter to Input Offset Voltage
 Parameter, Table 1 4
 Changed Offset Voltage Parameter to Input Offset Voltage
 Parameter, Table 2 6
 Changed Offset Voltage Parameter to Input Offset Voltage
 Parameter, Table 3 8
 Changes to EMI Rejection Ratio Section and Figure 102.....32
 Moved Figure 114.....38
 Changes to Current Noise Considerations Section41
 Added Long-Term Drift Section, Temperature Hysteresis
 Section, Figure 136, Figure 137, and Figure 138; Renumbered
 Sequentially51
 Changes to Ordering Guide.....52

3/2016—Rev. 0 to Rev. A

Changed DNC Pin to IC PinThroughout
 Changes to Figure 1 1
 Changes to Figure 3 and Table 6 10
 Changes to Figure 29 15
 Changes to Theory of Operation Section28
 Changes to Humidity Effects Section and Figure 112..... 36
 Added Power Supply Recommendations Section, Power
 Supply Considerations Section, Table 16, and Figure 133 to
 Figure 135..... 49

10/2015—Revision 0: Initial Version

SPECIFICATIONS

5 V NOMINAL ELECTRICAL CHARACTERISTICS

Supply voltage (V_{SY}) = 4.5 V, common-mode voltage (V_{CM}) = $V_{SY}/2$, $T_A = 25^\circ\text{C}$, unless otherwise specified. Typical specifications are equal to the average of the distribution from characterization, unless otherwise noted. Minimum and maximum specifications are tested in production, unless otherwise noted.

Table 1.

Parameter ¹	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit	
INPUT CHARACTERISTICS							
Input Bias Current ^{2, 3}	I_B	RH < 50%		<1	±20	fA	
		−40°C < T_A < +85°C, RH < 50%			±20	fA	
		−40°C < T_A < +125°C, RH < 50%			±250	fA	
Input Offset Current ³	I_{OS}	RH < 50%		<1	±20	fA	
		−40°C < T_A < +125°C, RH < 50%			±150	fA	
Input Offset Voltage ^{2, 4}	V_{OS}	$V_{CM} = 1.5\text{ V to }3\text{ V}$		+8	±40	μV	
		$V_{CM} = 1.5\text{ V to }3\text{ V}, 0^\circ\text{C} < T_A < 125^\circ\text{C}$		+9	±50	μV	
		$V_{CM} = 1.5\text{ V to }3\text{ V}, -40^\circ\text{C} < T_A < 0^\circ\text{C}$				±70	μV
		$V_{CM} = 0\text{ V to }3\text{ V}$				±150	μV
		$V_{CM} = 0\text{ V to }3\text{ V}$				±300	μV
Offset Voltage Drift ^{2, 4}	$\Delta V_{OS}/\Delta T$	0°C < T_A < 125°C		+0.13	±0.5	μV/°C	
		−40°C < T_A < 0°C		−0.7	±2.8	μV/°C	
Input Voltage Range	IVR		0		3	V	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 1.5\text{ V to }3\text{ V}$	92	114		dB	
		−40°C < T_A < +125°C	90			dB	
		$V_{CM} = 0\text{ V to }3\text{ V}$	73			dB	
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$ to V_{CM} , $V_{OUT} = 0.2\text{ V to }4.3\text{ V}$	120	143		dB	
		−40°C < T_A < +125°C	120			dB	
Input Resistance	R_{IN}	−40°C < T_A < +125°C		>100		TΩ	
Input Capacitance	C_{IN}			8		pF	
OUTPUT CHARACTERISTICS							
Output Voltage High	V_{OH}	$R_L = 10\text{ k}\Omega$ to V_{CM}	4.47	4.49		V	
		−40°C < T_A < +125°C	4.46			V	
		$R_L = 2\text{ k}\Omega$ to V_{CM}	4.4	4.45		V	
		−40°C < T_A < +125°C	4.38			V	
Output Voltage Low	V_{OL}	$R_L = 10\text{ k}\Omega$ to V_{CM}		10	30	mV	
		−40°C < T_A < +125°C			40	mV	
		$R_L = 2\text{ k}\Omega$ to V_{CM}		30	100	mV	
		−40°C < T_A < +125°C			120	mV	
Short-Circuit Current Source	I_{SC}			15		mA	
				−30		mA	
Sink							
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, $A_V = 1$		20		Ω	
POWER SUPPLY							
Power Supply Rejection Ratio	PSRR	$V_{SY} = 4.5\text{ V to }16\text{ V}$	130	150		dB	
		−40°C < T_A < +125°C	130			dB	
Supply Current	I_{SY}	$I_{OUT} = 0\text{ mA}$		0.9	1.3	mA	
		−40°C < T_A < +125°C			1.5	mA	
DYNAMIC PERFORMANCE							
Slew Rate	SR	$R_L = 10\text{ k}\Omega$, $C_L = 10\text{ pF}$, $A_V = 1$		1.4		V/μs	
Gain Bandwidth Product	GBP	$V_{IN} = 10\text{ mV rms}$, $R_L = 10\text{ k}\Omega$, $C_L = 10\text{ pF}$, $A_V = 100$		2		MHz	
Unity-Gain Crossover	UGC	$V_{IN} = 10\text{ mV rms}$, $R_L = 10\text{ k}\Omega$, $C_L = 10\text{ pF}$, $A_{VO} = 1$		2		MHz	

Parameter ¹	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
-3 dB Closed-Loop Bandwidth	f_{-3dB}	$V_{IN}=10$ mV rms, $R_L = 10$ k Ω , $C_L = 10$ pF, $A_V = 1$		6		MHz
Phase Margin	Φ_M	$V_{IN} = 10$ mV rms, $R_L = 10$ k Ω , $C_L = 10$ pF, $A_{VO} = 1$		62		Degrees
Settling Time to 0.1%	t_s	$V_{IN} = 0.5$ V step, $R_L = 10$ k Ω , $C_L = 10$ pF, $A_V = -1$		5		μ s
EMI Rejection Ratio of +IN	EMIRR	$V_{IN} = 100$ mV peak, $f = 400$ MHz		50		dB
		$V_{IN} = 100$ mV peak, $f = 900$ MHz		60		dB
		$V_{IN} = 100$ mV peak, $f = 1800$ MHz		80		dB
		$V_{IN} = 100$ mV peak, $f = 2400$ MHz		90		dB
NOISE PERFORMANCE						
Peak-to-Peak Voltage Noise	e_N p-p	$f = 0.1$ Hz to 10 Hz		4		μ V p-p
Voltage Noise Density	e_N	$f = 10$ Hz		80		nV/ \sqrt Hz
		$f = 1$ kHz		16		nV/ \sqrt Hz
		$f = 10$ kHz		14		nV/ \sqrt Hz
Current Noise Density	I_N	$f = 0.1$ Hz		0.07		fA/ \sqrt Hz
Total Harmonic Distortion + Noise	THD + N	$A_V = 1$, $f = 1$ kHz, $V_{IN} = 0.5$ V rms		0.003		%
				0.0045		%
GUARD BUFFER						
Guard Offset Voltage ^{2, 4, 5}	V_{GOS}	$V_{CM} = 1.5$ V to 3 V		15	100	μ V
		$V_{CM} = 1.5$ V to 3 V, $0^\circ\text{C} < T_A < 125^\circ\text{C}$			120	μ V
		$V_{CM} = 1.5$ V to 3 V, $-40^\circ\text{C} < T_A < 0^\circ\text{C}$			250	μ V
		$V_{CM} = 0.1$ V to 3 V			150	μ V
Guard Offset Voltage Drift ^{2, 4}	$\Delta V_{GOS}/\Delta T$	$0^\circ\text{C} < T_A < +125^\circ\text{C}$		0.18	1	μ V/ $^\circ\text{C}$
		$-40^\circ\text{C} < T_A < 0^\circ\text{C}$		1.4	7	μ V/ $^\circ\text{C}$
Output Impedance	Z_{GOUT}			1		k Ω
Output Voltage Range		$V_{GOS} < 150$ μ V	0.1		3	V
-3 dB Bandwidth	$f_{-3dBGUARD}$	$V_{IN} = 10$ mV rms, $C_L = 10$ pF		5.5		MHz

¹ These specifications represent the performance for $5\text{ V} \pm 10\%$ power supplies. All specifications are measured at the worst case 4.5 V supply voltage.

² The maximum specifications at $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ and $-40^\circ\text{C} < T_A < 0^\circ\text{C}$ are guaranteed from characterization.

³ RH is relative humidity (see the Humidity Effects section for more information).

⁴ The typical specifications are equal to the average plus the standard deviation of the distribution from characterization.

⁵ The guard offset voltage is the voltage difference between the guard output and the noninverting input.